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Date: January 21, 2008

To: United States Patent and Trademark Office
Examiner: Chen, Kin Chan; Art Unit: 1792

Fax: (571) 273-8300

Re: **Application Serial No.: 10/705,347**
Filing Date: 11/8/2003; First-Named Inventor: Labelle
Attorney Docket No.: 0180151

From: Farjami & Farjami LLP

Number of pages including the cover sheet: 13

Message:

Enclosed please find the Response to Final Office Action dated November 19, 2007.

Thank you.

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Attorney Docket No.: 0180151

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JAN 22 2008

In re Application of: **Labelle, et al.**

Serial No.: 10/705,347

Filed: 11/08/2003

For: **Method for Integrating a High-K Gate
Dielectric in a Transistor Fabrication
Process**

Art Unit: 1792

Examiner: Chen, Kin Chan

RESPONSE TO FINAL OFFICE ACTION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is in response to the *Final Office Action* dated November 19, 2007 in the
above-referenced patent application. Please enter and consider the following remarks.